FPGA-Based Data Processing using High-Level Synthesis on the Antarctic Demonstrator for the Advanced Particle-astrophysics Telescope (ADAPT)

Marion Sudvarg, Longhao Huang, Boran Yang, Roger Chamberlain, Jeremy Buhler
Leonardo Di Venere, Davide Serini, James Buckley, for the APT Collaboration

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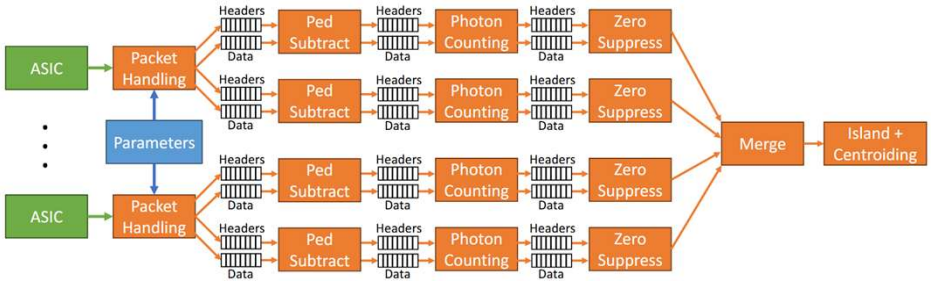
Abstract

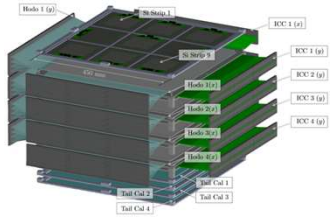
FPGAs are widely deployed on high-energy astrophysics telescopes to read out sensor data from front-end electronics. Across instruments, FPGA-based processing pipelines often have similar semantics and share common stages. However, diverse telescope designs require unique implementations of the constituent algorithms, and the logic is often rewritten from scratch for a new instrument. High-Level Synthesis (HLS) allows these algorithms to be implemented in a high-level language, enabling fast prototyping and deployment. This work presents an initial HLS library of common algorithms for deployment in particle astrophysics detectors. We apply it to the Antarctic Demonstrator for the Advanced Particle-astrophysics Telescope (ADAPT), an MeV–TeV gamma-ray/cosmic-ray instrument that combines a pair tracker and Compton telescope anticipated to fly on a high-altitude balloon during the 2026–27 Antarctic season.

The Computation Pipeline

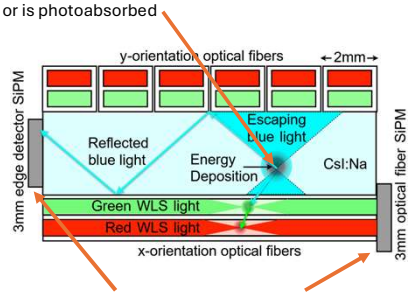


The Detector

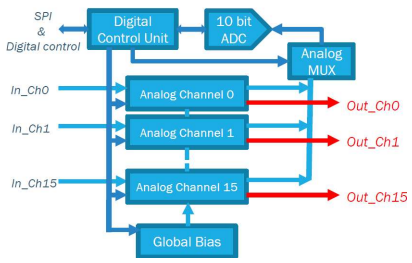
- 4 primary detector layers coupling an imaging CsI calorimeter (ICC) and scintillating fiber tracker hodoscope
- Each ICC layer has a 3x3 arrangement of 15 cm x 15 cm x 5 mm CsI:Na scintillating crystal
- Orthogonal 2mm wavelength shifting (WLS) fibers are bonded to the top and bottom of each ICC layer
- SiPM-based edge detectors improve light collection and calorimetry
- 4 additional closely-spaced CsI:Na tail counters have edge detectors but no WLS fibers



- In an ICC layer, a gamma-ray photon Compton scatters or is photoabsorbed



- WLS fibers and edge detectors read out by Hamamatsu S14160-3050HS SiPMs
- 3 WLS SiPM output signals combined into single SMART shaping preamplifier [1] channel



- 16-channel analog waveform digitizer ALPHA ASICs [2] or 32-channel HDSoC ASICs [3] sample response from SMART gain stages

FPGA Algorithms

Packet Handling

- Handles low-level interface with ASICs (supporting both the ALPHA or the HDSoC ASIC)
- Groups channels into sets of 16
- Inserts meta-data and data in two separate queues

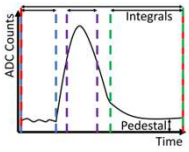
Pedestal Subtraction

- Normalize data samples relative to individual analog sample-and-hold cells in the ASIC chips

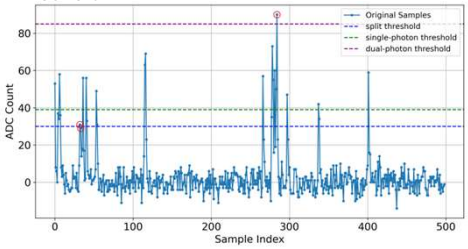
```
compute offset in ped[] from trigger
samples[] << input
for s in NUM_SAMPLES
  for c in NUM_CHANNELS
    output << samples[s,c] - ped[offset]
    update offset
  endfor
endfor
```

Photon Counting

Integration



Threshold



Hybrid

- Integrate over window around a sample above threshold

ADC to PE Conversion

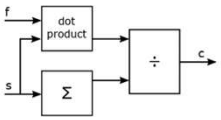
- Scale integral by area under single-PE impulse response
- Not required for threshold-based counting

Zero Suppression

- Values under a configurable threshold set to 0
- Removes spurious counts due to electronic noise or SiPM dark counts

Island Detection + Centroiding

- Identify adjacent non-zero fibers (f), called an island
- Compute dot product with signal values (s)



Performance

Achievable Throughput

- Events are individual gamma ray detections
- Pipeline performance is governed by slowest stage

Module	Throughput
Ped Subtract	383 000 events/s
Photon Counting (Integral)	369 000 events/s
Photon Counting (Hybrid)	64 000 events/s
Zero Suppress	4 350 000 events/s
Island + Centroiding	869 000 events/s

- Throughput is further limited by ASIC serial readout

Resource Usage

- Counts for 16 channels, percentage is for 80 channels

Module	LUTs	FFs
Packet Handling (5x)	8 820 (13%)	751 (0.9%)
Ped Subtract (5x)	785 (1.2%)	558 (0.7%)
Photon Counting: Hybrid (5x)	4 813 (7.4%)	3 671 (4.5%)
Zero Suppress (5x)	9 263 (14%)	2 115 (2.6%)
Island + Centroiding (1x)	37 043 (11%)	48 424 (12%)

Conclusions

- **We have presented a library of FPGA-based data preprocessing algorithms for high-energy telescopes**
- **They are implemented using HLS to ease adoption and prototyping effort**
- **Configured for the ADAPT suborbital gamma-ray/ cosmic-ray telescope they achieve >64K events/s (>300K for less robust photon counting techniques)**

Future Work

- **Further optimizations are desired in both speed and resource usage**
- **A wider set of available algorithms is also envisioned (e.g., 2-dimensional island detection and centroiding)**

References

[1] C. Aramo, E. Bissaldi, M. Bitossi et al., A SiPM multichannel ASIC for high Resolution Cherenkov Telescopes (SMART) developed for the pSCT camera telescope, *Nucl. Instrum. Methods Phys. Res. A* 1047 (2023).

[2] M. Kuwahara and G.S. Varner, Design and Development of Advanced Low Power Hybrid Acquisition (ALPHA) ASIC for Antarctic Demonstrator for the Advanced Particle-astrophysics Telescope (ADAPT), in *Proc. of Nucl. Science Symp., Medical Imaging Conf. and Int'l Symp. on Room-Temp. Semicond. Detectors*, 2023.

[3] L. Macchiarulo et al., Measurement results for the high density digitizer system on chip (HDSoC): A waveform digitizer for high density detectors, in *Proc. of Nuclear Science Symp. and Medical Imaging Conf.*, 2022.

For more details, please see our project webpage at this link →

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